REMARKS

This paper is responsive to the Office Action identified above, and is responsive in any other manner indicated below.

PENDING CLAIMS

Claims 1-24 were pending, under consideration and subjected to examination in the Office Action. Unrelated to any prior art rejection, appropriate claims have been amended in order to adjust a clarity and/or focus of Applicant's claimed invention. The amendments to the claims are unrelated to any prior art or scope adjustment, and are simply clarified claims in which Applicant is presently interested. At entry of this paper, Claims 1-24 will remain pending for further consideration and examination in the application.

35 USC §112, 1ST PARAGRAPH REJECTION - CLAIMS CLARIFIED

Claims 1-24 have been rejected under 35 USC §112, first paragraph, for the concerns listed within the section numbered "1" on page 2 of the Office Action. Traversal is appropriate. However, such rejection has been rendered moot by the present clarifying amendments to Applicant's claims, and accordingly, traversal arguments are not appropriate at this time. However, Applicant respectfully submits the following to preclude renewal of any such rejection against Applicant's clarified claims.

More particularly, with regard to the subject claim limitations of "a bulk capacitor with low equivalent series resistance connected between an output side of the ferrite bead and ground," attention is directed to Applicant's original specification

at page 5, lines 15-24, and especially lines 19-22 which explicitly state, "The key to this arrangement is...the use of a bulk decoupling capacitor with low equivalent series resistance." Page 5, line 24 through page 6, line 4, then goes on to describe an equivalence (low resistance) example where the bulk capacitor resistance is 0.8 Ohms and the ferrite bead resistance is 0.3 Ohms.

It is respectfully noted that the term "low equivalent series reistance" (sometimes called low ESR) is a specialized phrase in the capacitor art, and such specialized term is known to persons skilled in the art to which the present invention is directed. A simple search on the Internet using such specialized term turns up hundreds of hits.

In view of the explicit disclosure within Applicant's original specification of the "low equivalent series resistance" features/limitations, it respectfully submitted that the subject claim limitations do not represent new matter. Based upon the foregoing, reconsideration and withdrawal of the above-referenced rejection are respectfully requested.

ALL CLAIMS IN CONDITION FOR ALLOWANCE

In view of the fact that the above traversed rejection is believed to have been overcome, and in view of the fact that none of the presently pending claims have been rejected on a basis of prior art, it is respectfully submitted that all presently pending claims are now in condition for allowance. A Notice of Allowance with respect to the present application is respectfully requested.

GRATUITOUS OFFICE ACTION STATEMENTS GENERALLY TRAVERSED

The 11 June 2002 Office Action makes gratuitous statements (*e.g.*, on the top of page 3 of the Detailed Action) which are unconnected/unrelated to any presently pending rejection/objection. Applicant and the undersigned categorically traverse such statements, and also respectfully reserve the right to more explicitly traverse such statements should any statutory rejection/objection (connected to such statements) be made. That is, Applicant and the undersigned respectfully refrain from further unnecessary prosecution history estoppel comments regarding such statements unless and until a rejection or objection related thereto is made.

EXTENSIVE PROSECUTION NOTED

Applicant and the undersigned respectfully note the extensive prosecution which has been conducted to date with the present application, and thus Applicant and the undersigned would gratefully appreciate any considerations or guidance from the Examiner to help move the present application quickly to allowance.

ENTRY AFTER FINAL REJECTION

For all of the foregoing reasons, Applicant submits that the present paper should be entered since it places the rejected claims in condition for allowance by complying with the Examiner's requirements and/or amending and/or arguing the claims to distinguish such claims from the applied prior art.

Alternatively, this response should be entered since it presents the rejected claims in better form for consideration on appeal.

EXAMINER INVITED TO TELEPHONE

The Examiner is invited to telephone the undersigned attorneys at the local Washington, D.C. area telephone number 703-312-6600, to discuss an Examiner's Amendments or other suggested actions for accelerating prosecution and moving the present application to allowance.

CONCLUSION

In view of the foregoing amendments and remarks, Applicant respectfully submits that the claims listed above as presently being under consideration in the application are now in condition for allowance. Accordingly, early allowance of such claims is respectfully requested.

Applicant respectfully petitions the Commissioner for an appropriate extension of the period for response under 37 C.F.R. §1.136. Form PTO-2038 is attached, authorizing payment of the requisite Petition fee. Please charge any shortage in fees to ATSK Deposit Account No. 01-2135 (as No. 219.39043X00).

Respectfully submitted,

Paul J. Skwierawski, Registration No. 32,173
ANTONELLI, TERRY, STOUT & KRAUS, LLP
1300 North Seventeenth Street, Suite 1800
Arlington, VA 22209-3801
Telephone 703-312-6600
Facsimile 703-312-6666

ATTACHMENTS:
Appendix-Version With Markings
Form PTO-2038

APPENDIX - VERSION WITH MARKINGS TO SHOW CHANGES MADE IN THE CLAIMS:

Please amend the claims as follows. Note that the full text of all claims (including those not being amended within this paper) may also be included to provide the convenience of a complete set of claims for easy review:

1. (Twice amended) A circuit for removing noise on a voltage input line, comprising:

a ferrite bead connected in the voltage input line, the ferrite bead having a first resistance; and

a bulk capacitor with low equivalent series resistance connected between an output side of the ferrite bead and ground, [, the bulk capacitor having a substantially equivalent series resistance to the first resistance.]

2. (Amended) The circuit according to claim 1, wherein the capacitor is a D case tantalum bulk capacitor.

3. (Amended) The circuit according to claim 2, wherein the capacitor has the series resistance of approximately 0.8 Ohms.

4. (Amended) The circuit according to claim 1, wherein the ferrite bead has the first resistance of approximately 0.3 Ohms.

5. (Twice amended) A voltage supply device comprising:

a voltage source including a voltage regulator section producing a voltage output;

a ferrite bead connected at one side to the voltage output and forming at another side an output, the ferrite bead having a first resistance; and

a capacitor with low equivalent series resistance connected between the output and ground; [, the capacitor having a substantially equivalent series resistance to the first resistance;]

where switching regulator noise from the voltage regulator section is removable by the ferrite bead and capacitor.

6. (Amended) The voltage supply device according to claim 5, wherein the capacitor is a D case tantalum bulk capacitor.

7. (Amended) The voltage supply device according to claim 5, wherein the capacitor has the series resistance of approximately 0.8 Ohms.

8. (Amended) The voltage supply device according to claim 5, wherein the ferrite bead has the first resistance of approximately 0.3 Ohms.

9. (Twice amended) A method of removing switching regulator noise from a voltage supply line, comprising:

connecting a ferrite bead in the voltage input line, the ferrite bead having a first resistance; and

connecting a bulk capacitor with low equivalent series resistance between an output side of the ferrite bead and ground, [, the capacitor having a substantially equivalent series resistance to the first resistance.]

10. (Amended) The method according to claim 9, wherein the capacitor is a D case tantalum bulk capacitor.

11. (Amended) The method according to claim 10, wherein the capacitor has the series resistance of approximately 0.8 Ohms.

12. (Amended) The method according to claim 9, wherein the ferrite bead has the first resistance of approximately 0.3 Ohms.

13. (Twice amended) A voltage source for a clock circuit, comprising:

a voltage regulator having a regulator output;

a ferrite bead connected to the regulator output of the voltage regulator and having an output, the ferrite bead having a first resistance; and

a bulk capacitor with low equivalent series resistance connected to the output of the ferrite bead at one side and ground at another side; [, the bulk capacitor having a substantially equivalent series resistance to the first resistance;]

wherein the ferrite bead and capacitor act to remove switching regulator noise so as to produce an input voltage supply having a reduced switching regulator noise for the clock circuit.

14. (Amended) The voltage source according to claim 13, wherein the capacitor is a D case tantalum bulk capacitor.

15. (Amended) The voltage source according to claim 14, wherein the capacitor has the series resistance of approximately 0.8 Ohms.

16. (Amended) The voltage source according to claim 13, wherein the ferrite bead has the first resistance of approximately 0.3 Ohms.

17. The circuit according to claim 1, wherein the ferrite bead and the capacitor are provided in an "L" shaped filter configuration.

18. The circuit according to claim 1, wherein the ferrite bead and the capacitor form a resistor divider circuit to assist in noise signal removal.

19. The voltage supply device according to claim 5, wherein the ferrite bead and the capacitor are provided in an "L" shaped filter configuration.

20. The voltage supply device according to claim 5, wherein the ferrite bead and the capacitor form a resistor divider circuit to assist in noise signal removal.

21. The method according to claim 9, wherein the ferrite bead and the capacitor are provided in an "L" shaped filter configuration.

22. The method according to claim 9, wherein the ferrite bead and the capacitor form a resistor divider circuit to assist in noise signal removal.

23. The voltage source according to claim 14, wherein the ferrite bead and the capacitor are provided in an "L" shaped filter configuration.

24. The voltage source according to claim 14, wherein the ferrite bead and the capacitor form a resistor divider circuit to assist in noise signal removal.